Si-Ge interlayer having lateral edges which do not substantially extend beyond the lateral edges of the metal disilicide.--

REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the present Office Action, Claim 23 is objected to for the reason mentioned at Page 3 of the present Office Action. Applicants have amended Claim 23 in the manner proposed by the Examiner in the present Office Action. Specifically, in Claim 23, line 8, the term "said substrate" was replaced with the term "said exposed region of said substrate". This particular amendment to Claim 23 obviates the informality mentioned in the present Office Action. Reconsideration and withdrawal of the instant objection is thus respectfully requested.

The drawings are objected to under 37 C.F.R. §1.83(a) since the drawings allegedly do not show every feature of the invention specified in the claims. Specifically, the drawings do not show the exposed region specified in Claim 23. Applicants note that in the present Office Action, the Examiner has indicated that the suggested change in claim language, as performed above, would obviate the foregoing objection to the drawings. Since applicants have amended Claim 23, as proposed by the Examiner, the drawing objection has been obviated; therefore reconsideration and withdrawal of the drawing objection are respectfully requested.

Claims 29 and 30 stand rejected under 35 U.S.C. §112, first paragraph as allegedly containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors, at the time the application was filed, had possession of the claimed invention.

In response to this formal ground of rejection, applicants have canceled Claims 29 and 30, without prejudice or disclaimer. The cancellation of Claims 29 and 30 makes the formal rejection moot; therefore reconsideration and withdrawal thereof are respectfully requested.

In addition to the above amendments, applicants have also amended Claim 23 to positively recite that the electrical contact contains a metal disilicide which includes an additive or Ge. Support for this amendment to Claim 23 is found at Page 9, lines 7-22 and Page 12, lines 2-5 of the specification of the instant application.

Applicants have also added new Claims 36-39 which recite specific additives and the amount of additive that may be present in the metal disilicide layer. Support for these newly added claims is also found at Page 9, lines 7-22.

Applicants have additionally added new Claim 40 which positively recites that the lateral edges of the Si-Ge interlayer do not substantially extend beyond the lateral edges of the metal disilicide layer. Support for this newly added claim is found in the drawings, particularly FIG 1F, wherein Si-Ge interlayer 22 has lateral edges which do not extend beyond the lateral edges of metal dislicide 24.

Pursuant to 37 C.F.R. §1.121, applicants have attached a marked-up version of the claims showing the changes made by the present amendment. The attachment is captioned as "**MARKED-VERSION SHOWING CHANGES MADE**".

Claims 23, 25-27 and 31 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 5,710,450 to Chau, et al. ("Chau, et al.") and Wolf, "Silicon Processing for the VLSI Era, Vol. 2-Process Integration, Lattice Press: Sunset Beach CA, 1990, pp. 144-151 ("Wolf"). Claims 23, 25-27 and 31 also stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 6,121,100 to Andideh, et al. ("Andideh, et al.") and Wolf.

Applicants submit that claims of the present application are not obvious from the combined disclosures of Chau, et al. and Wolf or Andideh, et al. and Wolf since none of the applied references teaches or suggests applicants' claimed electrical contact that contains a first layer of *metal disilicide which includes an additive or Ge*, wherein the metal of the

disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and the exposed region of the substrate and the first layer are separated by a Si-Ge interlayer. That is, the applied prior art references do not teach or suggest a structure wherein the metal disilicide includes an additive or Ge, as is presently claimed.

The principal references to Chau, et al. and Andideh, et al. disclose semiconductor structures which include silicide regions located atop source/drain regions. The silicide regions of the prior art contain a refractory metal such as Ti or W. There is no teaching or suggestion in the principally applied references of a metal disilicide layer that includes an additive or Ge.

The secondary reference to Wolf does not alleviate the above defects in Chau, et al. and Andideh, et al. since the applied reference also does not teach or suggest a contact which includes a metal disilicide layer that contains an additive or Ge. In Wolf, various metal silicides are disclosed including refractory metal silicides, Group VIII metal silicides and Ti silicides. The applied reference does not teach or suggest the presence of an additive or Ge in any of their disclosed metal silicides. As such, the combined disclosures of Chau, et al. or Andideh, et al. with Wolf does not render applicants' claimed electrical contact obvious.

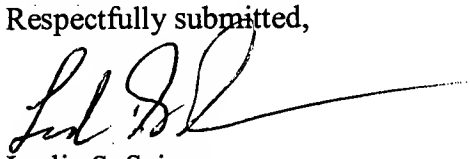
The §103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed metal silicides of the prior art to include an additive or Ge, as is presently claimed. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof are respectfully requested.

Applicants submit that new Claim 40 is not obvious from Chau, et al., Andideh, et al., and Wolf since none of the applied references teaches or suggests a structure in which the lateral edges of the Si-Ge interlayer do not substantially extend beyond the lateral edges of the metal disilicide. In Chau, et al. and Andideh, et al. the deposited SiGe layer extends well beyond the edges of silicide layer.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



Leslie S. Szivos
Registration No. 39,394

SCULLY, SCOTT, MURPHY & PRESSER
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343

LSS:gc

MARKED-VERSION SHOWING CHANGES MADE

IN THE CLAIMS:

Please cancel Claims 29 and 30, without prejudice or disclaimer, and please amend Claim 23 to read as follows:

23. (Amended) An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material; and

a first layer of metal disilicide which includes an additive or Ge, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a Si-Ge interlayer.

Please add the following new claims:

--36. The electrical contact of Claim 23 wherein said additive is selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

37. The electrical contact of Claim 36 wherein said additive is C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt or mixtures thereof

38. The electrical contact of Claim 37 wherein said additive is Si, Ti, V, Cr, Ni, Nb, Rh, Ta, Re, Ir or mixtures thereof.

39. The electrical contact of Claim 23 wherein said additive is present in said metal disilicide in an amount of from about 0.01 to about 50 atomic percent.--

40. An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material; and

a first layer of metal disilicide having lateral edges, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a Si-Ge interlayer, said Si-Ge interlayer having lateral edges which do not substantially extend beyond the lateral edges of the metal disilicide.--